

WHAT IS CLAIMED IS:

- 1    1. A self-directing bus amplifier circuit comprising:
  - 2        a. an input biased at a given voltage level;
  - 3        b. a tri-state amplifier having a first input
  - 4        terminal coupled to said biased input and having an
  - 5        output coupled to an output bus;
  - 6        c. a field effect transistor having a gate
  - 7        terminal coupled to said biased input, a source terminal
  - 8        coupled to ground potential, and a drain terminal coupled
  - 9        to an inhibiting input of said amplifier; and
  - 10      d. said drain terminal of said field effect
  - 11      transistor coupled to a source of voltage for bias
  - 12      thereof, such that when a signal is present on said input
  - 13      said field effect transistor turns OFF, which enables
  - 14      said tri-state amplifier so that said signal is passed
  - 15      through to said output bus.
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- 1    2. The circuit as in Claim 1 wherein said field effect
- 2        transistor is an N channel device.
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- 1    3. The circuit as in Claim 1 wherein said tri-state
- 2        amplifier is an OP AMP having an inhibiting input
- 3        thereof.
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- 1    4. The circuit as in Claim 1 wherein said input is
- 2        biased at a given level by means of a resistor coupled
- 3        between said input and source voltage.
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- 1    5. The circuit as in Claim 1 wherein said drain
- 2        terminal of said field effect transistor is biased at a
- 3        given level by means of a resistor coupled between said
- 4        drain terminal and source voltage.

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1 6. The circuit as in Claim 1 wherein a resistor is  
2 coupled between the output of said tri-state amplifier  
3 and said output bus for controlling the output impedance  
4 of said self-directing amplifier.

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1 7. The circuit as in Claim 1 wherein a gain network is  
2 coupled between a second input terminal of said tri-state  
3 amplifier and the output thereof.

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1 8. A self-directing bus amplifier circuit comprising:  
2       a. an input biased at a given voltage level;  
3       b. a tri-state amplifier having a first input  
4 terminal coupled to said biased input and having an  
5 output coupled to an output bus;  
6       c. a field effect transistor having a gate  
7 terminal coupled to said biased input, a source terminal  
8 coupled to ground potential, and a drain terminal coupled  
9 to an inhibiting input of said amplifier; and  
10      d. said drain terminal of said field effect  
11 transistor coupled to a source of voltage for bias  
12 thereof, such that when a signal is present on said input  
13 said field effect transistor turns OFF, which enables  
14 said tri-state amplifier so that said signal is passed  
15 through to said output bus;  
16      e. wherein said input is biased at a given level  
17 by means of a resistor coupled between said input and  
18 source voltage.

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1 9. The circuit as in Claim 8 wherein said field effect  
2 transistor is an N channel device.  
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1   10. The circuit as in Claim 8 wherein said tri-state  
2   amplifier is an OP AMP having an inhibiting input  
3   thereof.

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1   11. The circuit as in Claim 8 wherein said drain  
2   terminal of said field effect transistor is biased at a  
3   given level by means of a resistor coupled between said  
4   drain terminal and source voltage.

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1   12. The circuit as in Claim 8 wherein a resistor is  
2   coupled between the output of said tri-state amplifier  
3   and said output bus for controlling the output impedance  
4   of said self-directing amplifier.

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1   13. The circuit as in Claim 8 wherein a gain network is  
2   coupled between a second input terminal of said tri-state  
3   amplifier and the output thereof.

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1   14. A self-directing bus amplifier circuit comprising:  
2         a. an input biased at a given voltage level;  
3         b. a tri-state amplifier having a first input  
4   terminal coupled to said biased input and having an  
5   output coupled to an output bus;  
6         c. a field effect transistor having a gate  
7   terminal coupled to said biased input, a source terminal  
8   coupled to ground potential, and a drain terminal coupled  
9   to an inhibiting input of said amplifier; and  
10         d. said drain terminal of said field effect  
11   transistor coupled to a source of voltage for bias  
12   thereof, such that when a signal is present on said input  
13   said field effect transistor turns OFF, which enables

14 said tri-state amplifier so that said signal is passed  
15 through to said output bus;

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17 e. wherein said input is biased at a given level  
18 by means of a resistor coupled between said input and  
19 source voltage; and

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21 f. wherein said drain terminal of said field  
22 effect transistor is biased at a given level by means of  
23 a resistor coupled between said drain terminal and source  
24 voltage.

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1 15. The circuit as in Claim 14 wherein said field effect  
2 transistor is an N channel device.

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1 16. The circuit as in Claim 14 wherein said tri-state  
2 amplifier is an OP AMP having an inhibiting input  
3 thereof.

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1 17. The circuit as in Claim 14 wherein a resistor is  
2 coupled between the output of said tri-state amplifier  
3 and said output bus for controlling the output impedance  
4 of said self-directing amplifier.

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1 18. The circuit as in Claim 14 wherein a gain network is  
2 coupled between a second input terminal of said tri-state  
3 amplifier and the output thereof.

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1 19. In a video matrix routing switcher, a method for  
2 isolating a source of video signals on an input bus from  
3 an output bus, said method comprising:

4       a. providing an input biased at a given voltage  
5       level;

6       b. coupling a tri-state amplifier having a first  
7       input terminal between said biased input and an output  
8       bus;

9       c. coupling a gate terminal of a field effect  
10      transistor to said biased input, coupling a source  
11      terminal thereof to ground potential, and coupling a  
12      drain terminal to an inhibiting input of said amplifier;

13      d. coupling said drain terminal of said field  
14      effect transistor to a source of voltage for bias  
15      thereof;

16      e. providing a signal on said input, which turns  
17      off said field effect transistor thereby enabling said  
18      tri-state amplifier so that said signal is passed through  
19      to said output bus.

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1       20. The circuit method as in Claim 19 wherein said input  
2       is biased at a given level by means of coupling a  
3       resistor between said input and source voltage.

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1       21. The circuit method as in Claim 19 wherein said drain  
2       terminal of said field effect transistor is biased at a  
3       given level by means of coupling a resistor between said  
4       drain terminal and source voltage.

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1       22. The circuit method as in Claim 19 further comprising  
2       the step of coupling a resistor between the output of  
3       said tri-state amplifier and said output bus for  
4       controlling the output impedance of said self-directing  
5       amplifier.

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1   23. The circuit method as in Claim 19 further comprising  
2   the step of coupling a gain network between a second  
3   input terminal of said tri-state amplifier and the output  
4   thereof.